WHAT IS CLAIMED IS:

1. A latch circuit having an output, the output having a first state and a second state, the output being controllable by a first trigger signal and a second trigger signal, the latch circuit comprising:

a SET circuit;

a RESET circuit; and

wherein one condition from the group consisting of the following is true: 1) at the first state, a current is conducted by the SET circuit [such that] wherein the SET circuit is maintained such that a first switching threshold is obtainable by using the first trigger signal 2) at the second state, the current is conducted by the RESET circuit wherein the RESET circuit is maintained such that a second switching threshold is obtainable by using the second trigger signal and 3) a combination of 1 and 2, wherein the latch circuit forms a switching portion of an oscillator circuit.

2. A latch circuit having an output, the output having a first state and a second state, the output being controllable by a first trigger signal and a second trigger signal, the latch circuit comprising:

a SET circuit;

a RESET circuit; and

wherein one condition from the group consisting of the following is true: 1) at the first state, a current is conducted by the SET circuit wherein the SET circuit is maintained such that a first switching threshold is obtainable by using the first trigger signal 2) at the second state, the current is conducted by the RESET circuit wherein the

RESET circuit is maintained such that a second switching threshold is obtainable by using the second trigger signal and 3) a combination of 1 and 2, wherein the latch circuit forms a switching portion of a temperature-compensated oscillator circuit.

3. The latch circuit of claim 2, the temperature-compensated oscillator circuit further comprising level-shifting circuitry.

4. A latch circuit having at least one output, the output having a first state and a second state, the output being controllable by a first trigger signal and a second trigger signal, the latch circuit comprising:

a first latch transistor;

a second latch transistor coupled to the first latch transistor;

a SET transistor coupled to the first latch transistor; and

a RESET transistor coupled to the second latch transistor wherein one condition from the group consisting of the following is true: 1) at the first state, a current is conducted by the first latch transistor and the SET transistor wherein the SET transistor is biased such that a first threshold is obtainable by using the first trigger signal 2) at the second state, the current is conducted by the second latch transistor and the RESET transistor wherein the RESET transistor is biased such that a second threshold is obtainable by using the second trigger signal 3) a combination of 1) and 2), wherein the latch circuit forms a switching portion of an oscillator circuit.

5. A method of oscillating the output of an oscillator, the output having a first state and a second state, the oscillator including a latch, the latch including a first latch transistor, a second latch transistor, a SET transistor and a RESET transistor, the method comprising:

at the first state, conducting a first current in the first latch transistor and the SET transistor such that the SET transistor is biased at a point close to a first threshold;

at the second state, conducting the first current in the second latch transistor and the RESET transistor such that the RESET transistor is biased at a point close to a second threshold;

varying the output from the first state to the second state by providing a trigger current to raise the base of the SET transistor over a first threshold; and

varying the output from the second state to the first state by providing the trigger current to raise the base of the RESET transistor over a second threshold.

6. The method of claim 5 further comprising temperature compensating the oscillator.